

U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.
		M-15210 US 10/678,317	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	
(Use several sheets if necessary)		Yi Ding	
APR 26 2004 U.S. TRADEMARK OFFICE		Filing Date	Group
		October 3, 2003 2812	

## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
WP	AA	6,376,877	April 2002	Yu et al.			
WP	AB	6,448,606	Sept. 2002	Yu et al.			
WV	AC	6,417,047	July 2002	Isobe			
WP	AD	6,555,427	April 2003	Shimizu			
	AE						
	AF						
	AG						
	AH						
	AI						

## Foreign Patent Documents

## Translation

		Document	Date	Country	Class	Subclass	Yes	No
	AK							

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	
	AM	
	AN	
	AO	
	AP	
	AQ	

Examiner *K. Picardot* Date Considered *9/28/04*

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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				October 3, 2003	Unassigned			
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
70	AA	6,222,225	24 Apr. 2001	Nakamura et al.				
	AB	6,228,713	8 May 2001	Pradeep et al.				
	AC	6,323,085	27 Nov. 2001	Sandhu et al.				
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70	AJ	6,518,618	11 Feb. 2003	Fazio et al.				
Foreign Patent Documents								
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		Document	Date	Country	Class	Subclass	Yes	No
70	AK	2000-174242	23 Jun. 2000	JP				
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70	AL	Aritome, S. et al., "A 0.67um <sup>2</sup> Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) For 3V-only 256Mbit NAND EEPROMs," International Electron Devices meeting 1994, San Francisco, CA, December 11-14, 1994, pages 94-61 – 94-64.						
	AM	Keeney, Stephen N., "A 130nm Generation High Density Etox™ Flash Memory Technology, Intel, Corporation, Santa Clara, California, USA, 42 sheets.						
	AN	United States Patent Application No. 10/266,378 entitled "Floating Gate Memory Structures And Fabrication Methods," filed on October 7, 2002, Inventor: Chia-Shun Hsiao, Attorney Docket No. M-12200 US.						
	AO	United States Patent Application No. 10/262,785, entitled "Floating Gate Memory Fabrication Methods Comprising A Field Dielectric Etch With A Horizontal Etch Component," filed on October 1, 2002, Inventor: Yi Ding, Attorney Docket No.: M-12841 US.						
	AP	Silicon, Flash and Other Non-Volatile Memory Technologies, <a href="http://www.intel.com/research/silicon/flash.htm">http://www.intel.com/research/silicon/flash.htm</a> , September 12, 2002, pages 1-4.						
70	AQ	Patent Abstracts of Japan of JP 2000-174242.						
Examiner <i>RPiunay</i>		Date Considered <i>5/20/04</i>						
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